JEDEC STANDARD

A Procedure for Measuring P-Channel MOSFET Negative Bias Temperature Instabilities

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Introduction

Negative Bias Temperature Instabilities (NBTI) experienced by p-channel MOSFETs over time are an important reliability concern in modern microcircuits. The physical nature of the NBTI damage is not completely understood. It is believed that the NBTI damage is controlled by an electro-chemical reaction where holes in the P-MOSFET inverted channel interact with Si compounds (Si-H, Si-D, etc) at the Si-SiO2 interface to produce donor type interface states and possibly positive fixed charge. The relative contribution of interface states generation and positive fixed charge formation is very sensitive to the gate oxide process used in the technology. The electro-chemical reaction is strongly dependent on the gate vertical electric field and the temperature at stress. For this reason it is necessary to use the minimum oxide thickness allowed in the technology. The interface states generation and positive fixed charge formation may lead to substantial P-MOSFET parameter changes, in particular to an increase of threshold voltage (V_T). V_T is the most commonly used device parameter (as compared to transconductance or any drain current) to track the P-MOSFET degradation. This failure mechanism, which is found to be strongly thermally activated, may seriously affect the PMOS device reliability, particularly for analog blocks/designs where matching issues can be critical.

The material contained in this publication was formulated under the cognizance of the JEDEC JC-14.2 Subcommittee.

A PROCEDURE FOR MEASURING P-CHANNEL MOSFET NEGATIVE BIAS TEMPERATURE INSTABILITIES

(From JEDEC Board ballot JCB-04-47, formulated under the cognizance of the JC-14.2.2, Device Reliability Working Group.)

1 Scope

This document describes an accelerated stress and test methodology for measuring device parameter changes of a single p-channel MOSFET after Negative Bias Temperature Instability (NBTI) stress at dc bias conditions. This document gives a procedure to investigate NBTI stress in a symmetric voltage condition with the channel inverted ($V_{GS} < 0$) and no channel conduction ($V_{DS} = 0$).There can be NBTI degradation during channel conduction ($V_{GS} < 0$, $V_{DS} < 0$), however, this document does not cover this phenomena. Typically, p-channel MOSFET devices will display maximum parameter changes at elevated temperatures. The purpose of this document is to specify a minimum set of measurements so that valid comparisons can be made between different technologies, IC processes, and process variations in a simple, consistent and controlled way. The measurements specified should be viewed as a starting point in the characterization and benchmarking of the transistor manufacturing process.

The device parameters shift criteria specified in this document are to be used for comparison purposes only and should not be used as acceptance or rejection criteria. It is also important to realize that this procedure should not be interpreted as a means of predicting MOS IC failure rates. The impact of the p-channel MOSFET change on actual circuit performance is not addressed in this document. Though this procedure was developed for wafer level stressing, it is also applicable to packaged structures.

2 Applicable standards

ASTM F616-86, *Standard Method for Measuring MOSFET Drain Leakage Current.*

ASTM F617-86, *Standard Method for Measuring MOSFET Linear Threshold Voltage*.

ASTM F1096-87, *Standard Method for Measuring MOSFET Saturated Threshold Voltage*.

JESD77A, *Terms, Definitions, and Letter Symbols for Discrete Semiconductor and Optoelectronic Devices*.

JESD60A, *A Procedure for Measuring P-Channel MOSFET Hot-Carrier Induced Degradation at Maximum Gate CurrentUnder DC Stress*.

JESD28, *A Procedure for Measuring N-Channel MOSFET Hot-Carrier Induced Degradation Under DC Stress*.

3 Terms and definitions

bulk current, dc (I_B): The direct current into the bulk contact, which is the n-well current of a P-MOSFET.

bulk-source voltage (V_{BS}): The bulk-to-source voltage.

constant-current threshold voltage ($V_{T(ci)}$): The gate-source voltage at which the drain current is equal to a constant current, appropriate for a given P-MOSFET technology, times the ratio of gate width (W) to gate length (L). $V_{T(ci)}$ can be calculated using

$$V_{T(ci)} = V_{GS}\left(\text{at } I_D = I_{Do} \cdot \frac{W}{L}\right) \quad (1)$$

where: W and L are the gate width and gate length as printed on the wafer;

I_{Do} is typically –0.025 μA but another value may be selected for a given technology such that $V_{T(ci)}$ is in the subthreshold region of the device.

NOTE 1 The measurement technique must determine $V_{T(ci)}$ to within a 1-mV resolution. If the V_{GS} step size is larger than 1 mV, then a linear interpolation method may be used to achieve the 1-mV resolution.

NOTE 2 Typical dc bias voltages for the linear $V_{T(ci)}$ measurements are $V_{DS} = V_{DS(lin)}$, $V_{BS} = V_{BB}$. For the saturation $V_{T(ci)}$ the measurements conditions are $V_{DS} = -V_{DD}$ and $V_{BS} = V_{BB}$.

drain current, dc (I_D): The direct current into the drain contact.

drain leakage current ($I_{D(leak)}$): The drain current when the transistor is biased in its off state.

NOTE 1 $I_{D(leak)}$ may have contributions from channel off-state current, gate-induced drain leakage (GIDL), and drain-to-gate tunneling currents.

NOTE 2 Typical bias voltages for $I_{D(leak)}$ measurements are $V_{DS} = -V_{DD}$ and $V_{GS} = V_{BS} = V_{BB}$.

drain-source voltage (V_{DS}): The drain-to-source voltage.

extrapolated threshold voltage ($V_{T(ext)}$): The threshold voltage extrapolated from measurement of maximum slope ($g_{m(max)}$) of the I_D-V_{GS} curve, as described in ASTM F617-86. $V_{T(ext)}$ can be calculated using

$$V_{T(ext)} = V_{GS}(g_{m(max)}) - \frac{I_D(g_{m(max)})}{g_{m(max)}} \quad (2)$$

where: $V_{GS}(g_{m(max)})$ is the gate voltage at the point of the maximum slope of the I_D-V_{GS} curve;
$I_D(g_{m(max)})$ is the drain current at the point of the maximum slope of the I_D-V_{GS} curve;
$g_{m(max)}$ is the maximum slope of the I_D-V_{GS} curve in the linear region.

NOTE The bias voltages for $V_{T(ext)}$ measurements are $V_{DS} = V_{DS(lin)}$ and $V_{BS} = V_{BB}$.

3 Terms and definitions (cont'd)

gate current, dc (I_G): The direct current into the gate contact.

gate-source voltage (V_{GS}): The gate-to-source voltage.

linear drain current ($I_{D(lin)}$): The drain current when the transistor is biased in the linear region.

NOTE Typical bias voltages for $I_{D(lin)}$ measurements are $V_{DS(lin)}$ = -0.1 V, V_{GS} = -V_{DD} and V_{BS} = V_{BB}.

linear drain voltage ($V_{DS(lin)}$): The drain-to-source voltage for linear region measurements.

NOTE Typically, $V_{DS(lin)}$ = -0.1 V.

maximum operating junction temperature ($T_{J(max)}$): The maximum junction temperature specification for a given technology.

maximum linear transconductance ($g_{m(max)}$): The maximum slope of the I_D-V_{GS} curve in the linear region.

NOTE 1 The gate voltage shall be varied in increments no greater than 20 mV from below the turn-on voltage to a value great enough to ensure that the maximum slope point has been reached.

NOTE 2 The slope shall be calculated using a three-point linear least-squares best-fit algorithm as defined in ASTM F617-86.

NOTE 3 Typical bias voltages for $g_{m(max)}$ measurements are V_{DS} = $V_{DS(lin)}$ and V_{BS} = V_{BB}.

metal-oxide-semiconductor field-effect transistor (MOSFET): An insulated-gate field-effect transistor in which the insulating layer between each gate electrode and the channel is oxide material; the gate is metal or another highly conductive material.

NOTE See JESD77-B for further clarification of MOSFET terms.

NBTI: Negative bias temperature instability.

nominal bulk supply voltage (V_{BB}): The nominal bulk voltage for a given technology.

NOTE Typical V_{BB} = 0. If V_{BB} is not equal to zero, then V_{BB} for a P-MOSFET is positive.

nominal power supply voltage (V_{DD}): The nominal supply voltage for a given technology.

NOTE V_{DD} is positive.

n-well-to-source voltage ($V_{NW,S}$): The n-well-to-source voltage.

NOTE The n-well is the bulk of a P-MOSFET.

3 Terms and definitions (cont'd)

punch-through voltage (V_{PT}): The reverse-bias drain voltage applied to the drain terminal that results in significant drain-to-source current even though the transistor is biased in its off state.

NOTE 1 Punch-through is differentiated from junction breakdown in that the current path is from drain to source instead of from drain to substrate, as is the case of junction breakdown.

NOTE 2 Typical dc bias voltages for V_{PT} measurements on p-channel MOSFETs are V_{DS} at I_D = -1 µA and $V_{GS} = V_{BS} = V_{BB}$.

saturation drain current ($I_{D(sat)}$): The drain current when the transistor is biased in the saturation region.

NOTE Typical bias voltages for $I_{D(sat)}$ measurements are $V_{DS} = V_{GS} = -V_{DD}$ and $V_{BS} = V_{BB}$.

stress temperature (T_{stress}): The temperature at which the DUT is stressed during NBTI stress.

NOTE If only one temperature experiment is run, it is recommmended that the stress temperature be at least the maximum allowed during circuit operation or the burn-in temperature if burn-in is included.

test mode: The bias condition at which a given device parameter shift is monitored during the NBTI stress.

test temperature (T_{test}): The temperature at which the DUT is tested during the test of the device parameters during the NBTI stress.

time to target (t_{tar}): The time it takes under specific conditions for the value of a particular parameter to change by a specified amount or to a specified value.

NOTE For most other parameters, a change of 10% from the unstressed value is often used. For theshold voltage, a –10-mV change is often used. These values have been arbitrarily chosen, and no relationship to circuit failure is implied. Other criteria (e.g., 5% change from the unstressed value) may be used for a given technology.

4 Technical requirements

4.1 Equipment requirements

The measurement system must be capable of the simultaneous application of voltage and measurement of current at the gate, drain, and substrate contacts of the transistor. The system must be able to measure 100 pA with a resolution of 1 pA or better. The voltage overshoot during parametric measurements and stress must not exceed 1% of the applied voltage. If $I_{D(leak)}$ needs to be tracked as a device parameter during the stress, the measurement apparatus needs to be capable to measure less than $I_{D(leak)}$.

4 Technical requirements (cont'd)

4.2 Test structure requirements

A p-channel MOSFET fabricated on an n-type well should be used. The minimum allowed channel length and width (particularly for a Shallow Trench Isolation (STI) process) is recommended, but other channel lengths and widths can also be used. In addition MOSFETs with the minimum gate oxide thickness allowed by the technology must be evaluated. The gate, drain and source contacts of the transistor must be contacted; i.e., they shall not be floating. The n-well contact must be set during stress/test to the same bias conditions as in operation. To minimize parasitic voltage drops between the applied drain stress voltage and the device, the resistances from the probe pads to the device source, drain, and substrate should be minimized.

4.3 Measurement Requirements

The device should be set up at the wafer level on a probe station providing a stable platform via a vacuum chuck or as a packaged part in a test fixture. Chuck or fixture temperature shall be set at the stress temperature during stress and test. Once set, this temperature must be maintained to within +/- 2.0 °C of this set point for the duration of the test.

At the end of each NBTI stress interval, the stress is terminated and device parameters are measured. The stress time interval should be known to an accuracy of +/- 1% for stress time intervals over 1 second and 10% for stress intervals less than 1 second.

5 The NBTI stress test procedures

Figure 1 describes the NBTI stress test procedure.

Initial tests are used to select a "good" device (see 5.2) and to determine initial unstressed parameter values. If the device is determined to be "good," data is recorded and the stress cycle begins. During the stress cycle the device is biased using the selected stress bias and temperature conditions. The device parameter measurements are carried out at the stress temperature. Since changes in parameters typically exhibit a power law behavior the recommended stress intervals are at least 1/2 decade time-steps (see 5.4). After each stress cycle the selected device parameters are again determined, recorded and compared to the initial values. If the parameter degradation exceeds the target shifts (see 5.6), testing ends. Otherwise, another stress cycle is initiated. The sections below describe in greater detail the NBTI stress algorithm.

5 The NBTI stress test procedures (cont'd)

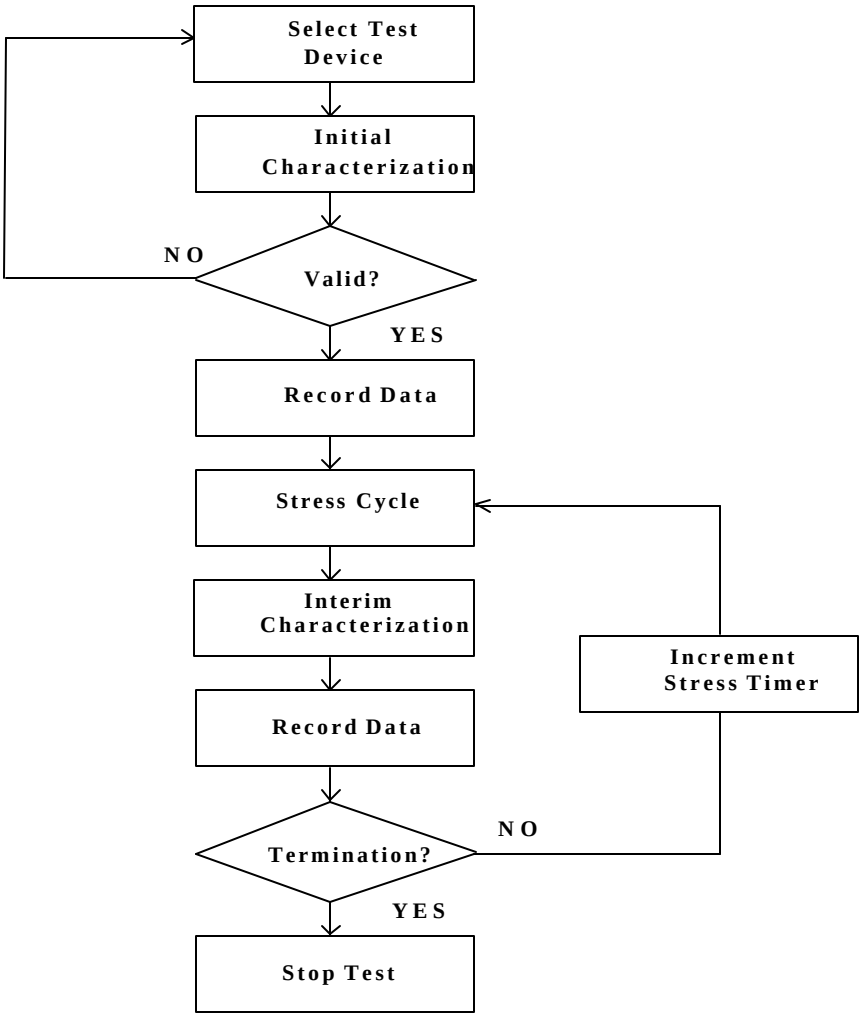

Figure 1 — The NBTI stress test procedure

5.1 Determining stress bias conditions

NBTI stressing should be performed under constant-voltage bias conditions at an elevated temperature. The NBTI stress configuration should be symmetric with no channel conduction. This means that during the stress, the gate terminal must be negatively biased (channel inverted), respect to the source and the drain ($V_{GS} < 0$), while $V_{DS} = 0$ (no channel conduction). The n-well to source ($V_{NW,S}$) should be set at conditions as required by the technology. As an example, NBTI stresses in CMOS bulk technologies should be run with $V_{NW,S} \geq 0$. In contrast, since Silicion On Insulator (SOI) P-MOSFETs may not have a body contact, the NBTI stress on SOI P-MOSFETs may need to be performed with a floating n-well. To determine the gate stress voltage, the I_G-V_G curve for the device must be examined. At stress, V_{GS} needs to be selected so that the vertical gate oxide electric field does not yield dielectric breakdown during NBTI. It is typical to use less than one-half the breakdown field from a ramped voltage test (see JESD35). If a gate protection diode is used, the diode should not be operated in avalanche regime.

5 The NBTI stress test procedures (cont'd)

5.2 Test devices

A transistor with gate, drain, and source leakage currents that meet the requirements of the process shall be used. Transistors selected for the NBTI stresses need key device parameters (such as V_T) within the technology/circuit requirements. In addition device dimensions such gate-oxide thickness, channel length and channel width need to be within the process requirements. Transistors used to define the NBTI stress bias conditions shall not be used for NBTI stress testing.

5.3 Initial characterization

Monitor device parameters in the test configurations critical to the specific circuit application, where the P-MOSFET is used. For typical CMOS applications device parameters such as $V_{T(ci)}$, $V_{T(ext)}$, $g_{m(max)}$, $I_{D(lin)}$, $I_{D(leak)}$ and $I_{D(sat)}$ are measured in linear and saturation condition. Depending on the specific circuit sensitivity to NBTI, other device parameters, such as gate leakage at operating voltage, off-state current, 1/f noise,etc. may also be measured. The selected device parameters shall be recorded, as these will be used for determining parametric shifts.

5.4 Stress cycle

The transistor will be stressed with the voltages determined in 5.1. The voltages shall be applied in the following order: V_{NW} (if applicable) first, V_D second and V_G last. The stress begins when V_G has been applied at the intended stress temperature. The stress continues until a stress time interval has been completed. Turning off the bias shall be done in the reverse order, with V_G first, V_D second and V_{NW} last.

Since the typical NBTI degradation follows a power law function with time in log-log scale, the recommended stress intervals are at least 1/2 decade time-steps. For example, the cumulative stress times could be 1, 3, 10, 30, 100, 300, 1000, 3000, 10000, 30000, and 100000 seconds. In this example, the device would be stressed for 1 second. After this stress interval, the device parameters are measured. The device would then be stressed for 2 additional seconds and the parameters again measured. The next stress interval would be 7 seconds. This procedure continues until stress termination occurs.

5.5 Interim characterization

The same device parameters selected for the initial characterization shall be used.

5.6 Stress termination

Each device shall be stressed until the selected device parameter reaches or exceeds the specified failure criterion. If a power law dependence with stress time is expected and the failure criterion is not achievable within the allowed stress time, the NBTI stress needs to be run until a linear log-log extrapolation to the failure criterion is possible (typically two time decades) (see 7.4).

6 Data analysis

Percent change for $g_{m(max)}$, $I_{D(sat)}$, $I_{D(leak)}$ and $I_{D(lin)}$, I_{off}(sat) is calculated from:

$$\mathbf{Y(t)} = \frac{\mathbf{P(t) - P(0)}}{\mathbf{P(0)}} * \mathbf{100} \quad (3)$$

where: P(0) is the initial parameter value.
P(t) is the parameter value at time t.

Relative shift for $V_{T(ci)}$ and $V_{T(ext)}$ is calculated from:

$$\mathbf{Y(t)} = \mathbf{P(t) - P(0)} \quad (4)$$

The absolute value of the change in each parameter is typically fitted to the following equation using a least-squares fit:

$$\left|Y(t)\right| = C \times t^{p} \quad (5)$$

where: $\left|Y(t)\right|$ is the absolute value of the NBTI shift with stress time of the parameter of interest. t is the cumulative stress time.

For each parameter analyzed, t_{tar} should be interpolated or extrapolated from the data based on the (C,p) values from this least-squares fit. Figure 2 shows an example of the use of equation 5. See applicable precautionary notes in 7.3 and 7.4.

7 Precautions

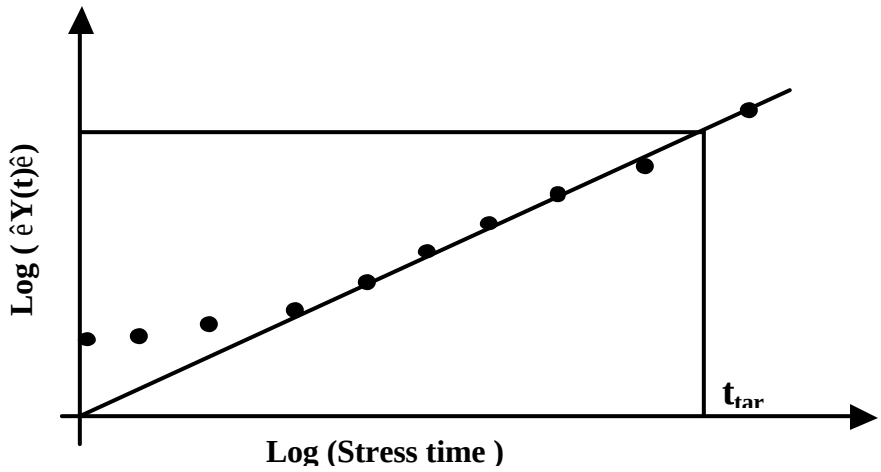

Figure 2 — Example of NBTI log-log fit to NBTI stress data.

While the procedures outlined above are quite straightforward, there are subtle effects that can cause significant errors. Listed below are some precautions that shall be followed to ensure correct implementation of the procedure.

7.1 Test sample

It is essential that devices used in NBTI stress testing should be unstressed devices. Test devices should not have been operated at a bias condition exceeding the nominal power supply voltage of the technology. Pre-stressed devices can show an appreciable shift in t_{tar} when compared to unstressed parts. Depending on the measured variability of the NBTI shifts for a given device an adequate sample size is required to achieve a given statistical confidence level.

7.2 Stress

Since the change in parameters is a sensitive exponential function of applied stress voltage, it is essential that the correct stress bias voltage be applied to the device under test. Discrepancies can arise due to high series resistance caused by poor probe-to-pad contact or from device short circuits leading to power supply compliance limitations. It must be determined that the MOSFET gate is not short-circuited during the stress.

7.3 NBTI recovery during interim measurements

Certain technologies have shown partial parameter recovery once stress biasing is removed. Since the amount of this recovery is strongly dependent on the technology to be evaluated and stress conditions (Gate Voltage/Temperature at stress) it is necessary to quantify this phenomenon during stress and at use conditions. In addition the estimate of t_{tar} must take the effect of NBTI recovery into account, particularly in a product application.

7 Precautions (cont'd)

7.3 NBTI recovery during interim measurements (cont'd)

To minimize the effect of the NBTI recovery during the interim measurements it is recommended to minimize the off stress time ($T_{off\text{-}stress}$) between the termination of the NBTI stess and the beginning of device parameters measurements. A long off stress time may result in significant parameter recovery leading to significant errors in the estimated NBTI degradation. Precautions should be taken when making multiple parametric measurements since different levels of relaxation may incur during the measurement time interval.

The length of the off stress time should be reported. Figure 3 shows the effect of the NBTI recovery during the off stress condition before the beginning of the interim measurements.

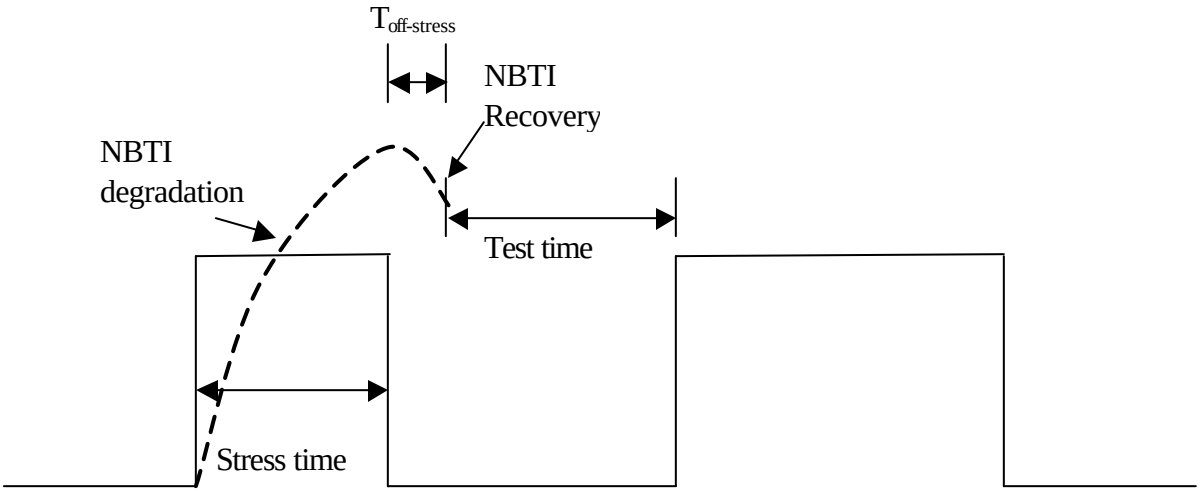

Figure 3 — NBTI recovery during Toff-stress

7.4 t_{tar} estimate

It is expected that the degradation of the selected P-MOSFET parameters during an NBTI stress follows a power law dependence with stress time. That is, the change of a given parameter of interest versus the stress time follows a straight line on a log-log plot. This is not always the case, possible saturation of the device parameter shift may take place during the stress. For example a superposion of two different power law regimes may occur. The slope of the log-log degradation curve can vary with increasing stress time (see Figure 4). Since the NBTI sensitivity to these saturation effects can vary from technology to technology and from process to process, it is necessary to take these effects into account when fitting degradation data. For this reason it is necessary to verify that, for the gate voltage and temperature stress condition of interest, the stress time is extended to verify the evolution of the shift up to t_{tar}. If t_{tar} is expected to fall in the linear region of the log-log scale then t_{tar} should be determined by using a power law fit. At a minimum the power law extrapolation should be based on the last two time decades. If the stress voltage is relatively low, the first few degradation measurements may produce parameter changes that are smaller than the test equipment can resolve. These data points should not be included in the data analysis.

7 Precautions (cont'd)

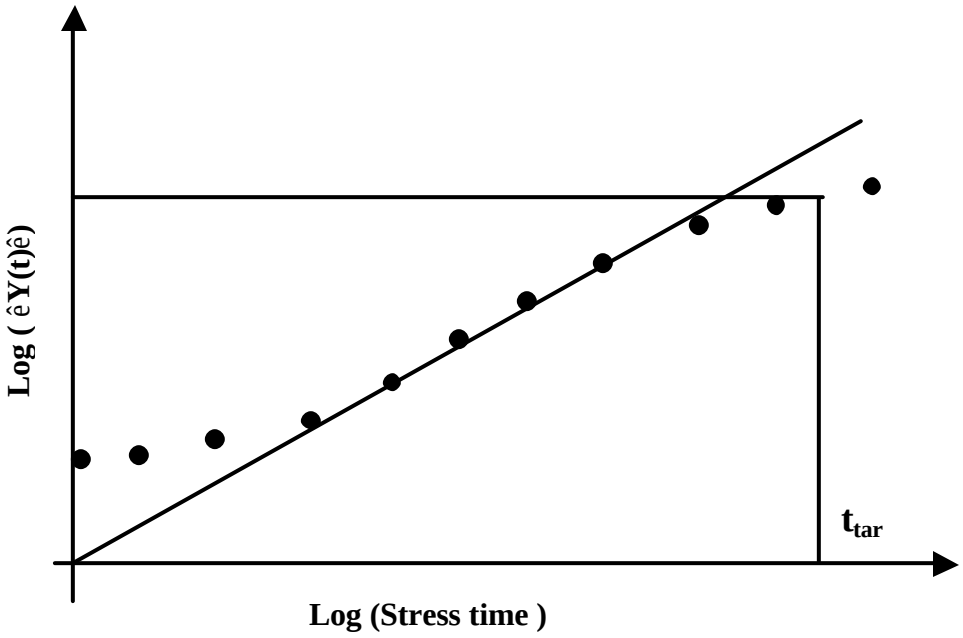

Figure 4 — Example of NBTI degradation showing t_{tar} in the saturation region.

8 Required reporting

As a minimum, the following information relevant to the p-channel MOSFET NBTI measurement should be reported.

8.1 Test transistor identification

Provide information sufficient to uniquely identify the MOSFET tested. (Lot identifications, Wafer identifications, chip location in the wafer).

8.2 Technology/process feature

Key elements of the P-MOSFET device design such as Gate oxide process, source/drain engineering etc.

8.3 V_{DD}, V_{BB}

The nominal power supply and bulk voltage for the technology under investigation.

8.4 $T_{J(max)}$

The maximum junction temperature specified for the technology under consideration.

8 Required reporting (cont'd)

8.5 MOSFET channel length and width

The final gate dimensions as printed on the wafer for the p-channel MOSFET under test.

8.6 MOSFET gate oxide thickness

The gate oxide thickness of p-channel MOSFET under test.

8.7 V_{NW} at stress

The MOSFET nwell-source voltage applied during stress.

8.8 V_{GS} at stress

The MOSFET gate-source voltage applied during stress.

8.9 Stress and test temperature

The temperature at which the DUT has been stressed during the NBTI stress.
It is assumed that the test temperature is the same as the stress temperature.

8.10 Initial values of selected device parameters

The initial (pre-stress) values of the selected device parameters in the appropiate test mode condition. For typical CMOS application $I_{D(lin)}$, $g_{m(max)}$, $V_{T(ci)}$, $V_{T(ext)}$, $I_{D(sat)}$, $I_{D(leak)}$ should be reported in linear and saturation forward..

8.11 t_{tar} for$V_{T(ci)}$ or $V_{T(ext)}$

This is the calculated time to reach the specified failure criterion for the selected device parameter (see definitions). For typical CMOS application at least the threshold voltage parameter and each of the six required parameters should be reported if possible.

8.12 Total stress time

The total cumulative stress time.

8.13 Off stress time

The off state measurement time.

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